REMARKS

Claims 1, 4, 5, 8-17, 19, 20, 22, 23, 25, 26, 28, 29, 31, 32, 34 and 35 are pending in this application. By this Amendment, claims 1, 4 and 14 are amended. No new matter is added by these amendments. Claims 2, 3, 6, 7, 18, 21, 24, 27, 30, 33 and 36 are canceled without prejudice to, or disclaimer of, the subject matter recited in those claims. Reconsideration of the application based upon the above amendments and the following remarks is respectfully requested.

The Office Action, in paragraph 3, objects to claim 1 for informalities. Claim 1 is amended to obviate this objection. Accordingly, withdrawal of the objection to claim 1 for informalities is respectfully requested.

The Office Action, in paragraphs 4-13, rejects claims 1-36 under 35 U.S.C. §103(a) as being unpatentable over varying combinations of U.S. Patent Nos. 6,567,484 to Hirota et al. (hereinafter "Hirota"), 4,672,639 to Tanabe et al. (hereinafter "Tanabe"), 4,975,702 to Bazes, 5,517,155 to Yamauchi et al. (hereinafter "Yamauchi"), 5,796,360 to Wenelrup, and 6,477,181 to Fujimori et al. (hereinafter "Fujimori"). The Applicant respectfully traverses these rejections.

The Office Action asserts that Bazes teaches when a set-up time of the first to N-th holding circuits is TS, a hold time of the first to N-th holding circuits is TH, and a period of each of the first to N-th clocks is T, number of clocks N of the first to N-th clocks is such that: $N \leq [T/(TS + TH)]$ (where [X] is a maximum integer that does not exceed X), as positively recited in amended claim 1. Specifically, the Office Action asserts that Bazes, in col. 6, first paragraph, teaches the resolution can be improved to Tr/N, and that there is a specified set up time, T_S, and hold time, T_H, for any clock device, and that it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the prior

art references of Hirota and Tanabe in establishing the equation of $N \leq [T/(T_S + T_H)]$. This assertion is incorrect.

Bazes teaches Tr/N indicates a resolution and not a relationship between the setup time, TS, and the hold time, TH, in a general circuit. Bazes is silent with respect to any relationship between T_R/N and setup and hold times. Therefore, Bazes does not explicitly teach all of the features as recited in the subject matter of pending claim 1.

In asserting that T_R/N must inherently be $\geq T_S + T_S$ (para. 5 of the Office Action), the Office Action is exercising nothing but impermissible hindsight. There is nothing in the disclosure of Bazes that teaches, or would have suggested, the relationship between the resolution (T_R/N) and the setup and hold times.

MPEP §2142 states, "the Examiner bears the initial burden of factually supporting any prima facie conclusion of obviousness." Additionally, §2142 states, "to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all of the claim limitations." Applicant submits that this standard is not met, as further discussed below.

Further clarifying "suggestion or motivation," the Federal Circuit has held that 35 U.S.C. §103 requires assessment of the invention "as a whole." Specifically, "this 'as a whole' assessment of the invention requires a showing that an artisan of ordinary skill in the art at the time of the invention, confronted by the same problems as the inventor and with no knowledge of the claimed invention, would have selected the various elements from the prior art and combine them in the manner claimed." *Ruiz v. AB Chance Co.* 357 F.3d 1270, 69 USPQ2d 1686 (Fed. Cir. 2004). The Federal Circuit went on to state, "[i]n other words,

§103(a) requires some suggestion or motivation, before the invention itself, to make the new combination." *Id.*

In addition to the arguments discussed above, the Office Action fails to make a *prima facie* case of obviousness for at least the following additional reasons. The "as a whole" instruction in Title 35 prevents evaluation of the invention part by part. Ruiz. Without this important requirement, an obviousness assessment might successfully break an invention into its component parts, then find a prior art reference corresponding to each component. *Id.* This line of reasoning would import hindsight into the obviousness determination by using the invention as a roadmap to find its prior art components. Further, this improper method would discount the value of combining various existing features or principles in a new way to achieve a new result-often the essence of an invention."

Applicant submits that one of ordinary skill in the art, would not have modified the applied prior art references, as enumerated above, in some permissible combination with Bazes, for at least the following reasons. A person skilled in the art generally increases the number of clocks, N, when a transfer rate is high, as in a high speed serial transfer, *e.g.*, USB. Specifically, a person skilled in the art considers that the amount of detected information is increased by increasing the number of clocks, N, whereby an appropriate sampling clock can be generated. Therefore, Bazes discloses a method in which the amount of sampling information is increased by increasing the number of clocks and sampling data using the clocks, and the change point is then calculated based on the sampling information. This is evidenced by the fact that Bazes sets the number of clocks, to 16 or 31 (col. 4, lines 35-40 and col. 6, lines 9-12). Additionally, Bazes employs a complicated calculation circuit, as illustrated in Fig. 2, to calculate the change point. This method, as taught by Bazes, results in an increase in the number of holding circuits and the like due to an increase in the number of clocks, whereby the circuit scale is increased.

The subject matter of the pending claims recites the number of clocks being set at N is $\leq$ or = [T/(TS + TH)]. Specifically, while a person skilled in the art would traditionally increase the number of clocks in order to deal with a high-speed transfer, the pending claims recite setting the number of clocks, N, at [T/(TS + TH)] or less. Additionally, the number of holding circuits can be reduced by setting the clocks, at $N \leq [T/(TS + TH)]$, whereby the circuit scale can be reduced. Therefore, the applied prior art references of Hirota, Tanabe, Yamauchi, Wenelrup and Fujimori, in any permissible combination with Bazes, failed to teach the subject matter as recited in amended claim 1. Specifically, that a set up time of the first two N-th holding circuits is T_S, a hold time of the first two N-th holding circuits is T_H, and a period of each of the first two N-th clocks is T, the number of clocks of the first two N-th clocks is such that: $N \leq [T/(TS + TH)]$ (where [X] is a maximum integer that does not exceed X).

For at least the above reasons, the applied prior art references in any permissible combination, cannot reasonably be considered to have suggested the combinations of all the features recited in at least independent claims 1 and 10. Further, claims 2-9 and 11-36 would also not have been suggested by the applied prior art references for at least the respective dependence of these claims, directly or indirectly, on allowable independent claims 1 and 10, as well as for the separately patentable subject matter that each of these claims recites.

Accordingly, reconsideration and withdrawal of the rejections of claims 1-36 under 35 U.S.C. §103(a) as being unpatentable over some combination of the applied prior art references, as enumerated above, are respectfully requested.

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of the claims are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

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